

1 VIDEO SIGNAL PROCESSOR  
23 BACKGROUND OF THE INVENTION  
4

## 5 1. Field of the Invention

6 The present invention relates to a video signal  
7 processor for providing the display, on a monitor screen,  
8 of both a video picture and at least one graphical  
9 representation of an associated signal characteristic, such  
10 as a video waveform, a vector diagram, an audio level  
11 display and an audio phase display.

12

## 13 2. State of the Art

14 Video signal processors are known in which a normal  
15 definition video signal is processed in order to provide a  
16 display of the video picture on part of a monitor screen,  
17 and graphical representations of associated signal  
18 characteristics on other parts of the same monitor screen.  
19 Typically the picture is displayed in one quarter of the  
20 screen, whilst a video waveform is displayed in a second  
21 quarter of the screen, a vector diagram is displayed in a  
22 third quarter of the screen, and audio level and phase  
23 information is displayed in graphical form in a fourth  
24 quarter of the screen.

1  
2       Where the normal definition video signal is processed  
3 for display on a normal definition monitor, because the  
4 picture is displayed at a quarter of its original size, it  
5 is displayed at a reduced resolution. The alternative is to  
6 process the normal definition video signal for display on a  
7 high resolution computer monitor: this preserves the  
8 original picture resolution but the interlaced fields of  
9 the incoming normal definition video signal must be de  
10 interlaced for display on the computer monitor and this  
11 creates undesirable artifacts in the processed signal and  
12 accordingly in the display.

13

14                   SUMMARY OF THE INVENTION

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16       In accordance with the present invention, there is  
17 provided a video signal processor which comprises an input  
18 for receiving an input video signal of a first definition,  
19 resizing means for processing the input video signal to  
20 provide a picture component signal corresponding thereto,  
21 analyzing means for processing the input video signal to  
22 provide a measurement component signal representing a  
23 graphical representation of at least one characteristic  
24 associated with the input video signal, a video signal

1 generator for generating a background video signal of a  
2 second definition, and means for combining the picture  
3 component signal and the measurement component signal into  
4 the background video signal to provide an output video  
5 signal of the second definition.

6

7       The signal processor is accordingly able to process a  
8 normal definition video signal for the display of the  
9 picture in part of a high definition monitor screen, whilst  
10 displaying, in another part of the screen, a graphical  
11 representation of at least one characteristic of the video  
12 signal.

13

14       Preferably, the video signal processor is arranged so  
15 that the picture will be displayed in one quarter of the  
16 monitor screen, with a video waveform, a vector diagram and  
17 audio information displayed in the other quarters of the  
18 screen.

19

20       Preferably, the input video signal (normal definition)  
21 will consist of a first plurality of horizontal lines (e.g.  
22 625 lines) made up of two interlaced fields, and the output  
23 video signal (high definition) will consist of a greater

1 number of horizontal lines (e.g. 1125 lines) made up of two  
2 interlaced fields.

3

4 It will be appreciated that the picture as displayed  
5 on the high definition monitor screen will, despite its  
6 reduced size, maintain its normal resolution.

7

8 Additional objects and advantages of the invention  
9 will become apparent to those skilled in the art upon  
10 reference to the detailed description taken in conjunction  
11 with the provided figures.

12

#### 13 BRIEF DESCRIPTION OF THE DRAWINGS

14

15 FIGURE 1 shows a display device that displays a multi-  
16 part video signal provided by a video signal processor; and

17

18 FIGURE 2 is a block diagram of a video signal  
19 processor in accordance with the present invention.

20

21 FIGURE 3 is a block diagram of an exemplary video  
22 signal processor in accordance with the present invention.

23

## 1            DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2

3            Referring to Figure 1 of the drawings, a video signal  
4 processor typically process an incoming video signal to  
5 generate an output video signal which creates a multi-part  
6 display on a monitor screen, which includes four quarters  
7 as shown. In one quarter A, the incoming video signal is  
8 displayed. In a second quarter B, one or more video  
9 waveforms are displayed. In a third quarter C, one or more  
10 vector diagrams are displayed. In the fourth quarter D,  
11 audio level and audio phase information is displayed in  
12 graphical form.

13

14           Referring to Figure 2, a video signal processor in  
15 accordance with the present invention processes an incoming  
16 video signal S with standard definition to provide an  
17 output video signal S' with high definition that suitable  
18 for display on a high definition display device in a manner  
19 shown in Figure 1. Such standard definition video signals  
20 typically provide interlaced fields of 625 (or 525)  
21 horizontal lines per field at the desired field rate. For  
22 example, the standard definition video signal S may have a  
23 PAL format having 625 interlaced horizontal lines per field  
24 (e.g., two interlaced fields of 312.5 lines each) at a 50

1    Hz field rate. The standard definition video signal may  
2    also have an NTSC format having 525 interlaced horizontal  
3    lines per field (e.g., two interlaced fields of 262.5 lines  
4    each) at a 60 Hz field rate. These exemplary standard  
5    definition video signal formats are supported by a wide  
6    variety of commercially available standard definition  
7    televisions and other standard definition video display  
8    devices.

9  
10       The high definition output video signal S' produced by  
11    the video signal processor has a high definition format  
12    that is suitable to drive a progressive scan (i.e., non-  
13    interlaced) display device at a resolution more than 600  
14    lines per field at a desired field rate (typically 50 Hz or  
15    60 Hz), or is suitable to drive an interlaced scan display  
16    device at a resolution of more than 1000 lines per field at  
17    a desired field rate. The high definition output video  
18    signal S' may have a high definition format of 1125  
19    interlaced horizontal lines per field (e.g., two interlaced  
20    fields of 562.5 lines each) at a desired field rate  
21    (typically 50 Hz or 60 Hz). In another example, the high  
22    definition output video signal S' may have a high  
23    definition format of 1080 interlaced horizontal lines per  
24    field (e.g., two interlaced fields of 540 lines each) at a

1 desired field rate (typically 50 Hz or 60 Hz). In yet  
2 another example, the high definition output video signal S'  
3 may have a high definition format of 720 progressive  
4 horizontal lines per field (e.g., each field includes 720  
5 lines) at a desired field rate (typically 50 Hz or 60 Hz).  
6 In yet another example, the high definition output video  
7 signal S' may have a high definition format of 1080  
8 progressive horizontal lines per field (e.g., each field  
9 includes 1080 lines) at a desired field rate (typically 50  
10 Hz or 60 Hz). These exemplary high definition video signal  
11 formats are supported by a wide variety of commercially  
12 available high definition televisions and other high  
13 definition video display devices.

14

15 The video signal processor includes a video signal  
16 generator G which generates a background signal V of high  
17 definition format (i.e. 1125 horizontal lines made up of  
18 two interlaced fields of 562.5 lines each). Preferably,  
19 the high definition background signal V comprises a  
20 blanking (e.g., black) video signal.

21

22 The video signal processor further comprises a  
23 resizing circuit R which receives the standard resolution  
24 incoming video signal S and processes the input video

1 signal S to provide a picture component signal P, which  
2 represents a reduced-size (i.e. quarter size) picture  
3 corresponding to the incoming video signal S. The  
4 processor also comprises a signal measurement or analysis  
5 circuit M which also receives the incoming video signal S  
6 and, from this, derives a measurement (or analysis) signal  
7 W which represents a video waveform, vector diagram and  
8 audio information display. Details of circuitry suitable  
9 for realizing the resizing circuit R and the signal  
10 measurement circuit M are set forth in detail in U.S.  
11 Patents No. 5,166,791 and 6,069,607 as well as UK Patent  
12 Application GB2183420, incorporated by reference herein in  
13 their entirety.

14

15 The video signal processor further comprises an output  
16 circuit O which combines the component signals V, P and O  
17 (by superimposing the picture component signal P and  
18 measurement signal O onto the high definition background  
19 signal V) to form the output video signal S' with high  
20 definition.

21

22 In use, the output video signal S' is fed to a high  
23 definition display device to create a display of the form  
24 shown in Figure 1. The picture (derived from the picture



1 component signal P) is displayed of reduced (quarter) size,  
2 but it will be appreciated that its resolution will be  
3 maintained, and will correspond with the resolution of the  
4 picture created had the incoming video signal S been fed  
5 directly to a lower definition display device, for display  
6 of the picture full-size on that lower-definition display  
7 device.

8  
9 Fig. 3 is a block diagram illustrating an exemplary  
10 embodiment of the video signal processor of Fig. 2. It  
11 includes resize circuitry 310 that receives the standard  
12 resolution input video signal S and processes the input  
13 video signal S to generate and store a picture component  
14 signal P, which includes an array of RGB pixel data values  
15 that represent a reduced-size (i.e. quarter size) picture  
16 corresponding to the incoming video signal S. The video  
17 signal processor also comprises a signal measurement  
18 circuit 312 which also receives the standard resolution  
19 video signal S and, from this, derives and stores a  
20 waveform component signal W, which includes separate arrays  
21 of RGB pixel data values that represent a video waveform, a  
22 vector diagram and audio information display, respectively.  
23 Details of circuitry suitable for realizing the resizing  
24 circuitry 310 and the signal measurement circuit 312 are

1 set forth in detail in U.S. Patents No. 5,166,791 and  
2 6,069,607 as well as UK Patent Application GB2183420,  
3 incorporated by reference above in their entirety.

4

5 The video signal processor includes a video signal  
6 generator 314 that generates a background signal V of high  
7 definition format (i.e. 1125 horizontal lines made up of  
8 two interlaced fields of 562.5 lines each). Preferably,  
9 the high definition background signal V comprises a  
10 blanking video signal (e.g., an RGB signal representing a  
11 blank (or black) color level).

12

13 A high definition timing signal generator 316  
14 generates timing signals that are used to scan/display a  
15 high definition video signal on a high resolution display  
16 device. These timing signals include a high definition  
17 pixel clock signal which represents transitions between  
18 pixels in the high definition video signal, a high  
19 definition horizontal synchronization signal which  
20 represents transitions between lines in the high definition  
21 video signal, and a high definition vertical  
22 synchronization signal that represents transitions between  
23 fields in the high definition video signal.

24

1       The timing signals generated by the timing signal  
2 generator 316 are provided to control circuitry 318, which  
3 analyzes these timing signals to ascertain if such signals  
4 correspond to particular portions of a high resolution  
5 display frame as follows. In the event that such timing  
6 signals correspond to a portion of a high resolution  
7 display frame in the top-left quadrant A, the control  
8 circuitry 318 cooperates with readout circuitry 320 and  
9 switch 324 to read out the picture component signal P  
10 generated and stored by the resize circuitry 310 for output  
11 as part of the high definition output video signal S'.  
12 In the event that such timing signals correspond to a  
13 portion of a high resolution display frame in the bottom-  
14 left quadrant B, the control circuitry 318 cooperates with  
15 readout circuitry 322 and switch 324 to read out the  
16 waveform image signal generated and stored by the  
17 measurement circuitry 312 for output as part of the high  
18 definition output video signal S'. In the event that such  
19 timing signals correspond to a portion of a high resolution  
20 display frame in the bottom-right quadrant C, the control  
21 circuitry 318 cooperates with readout circuitry 322 and  
22 switch 324 to read out the vector waveform signal generated  
23 and stored by the measurement circuitry 312 for output as  
24 part of the high definition output video signal S'.

1 In the event that such timing signals correspond to a  
2 portion of a high resolution display frame in the top-right  
3 quadrant D, the control circuitry 318 cooperates with  
4 readout circuitry 322 and switch 324 to read out the audio  
5 information signal generated and stored by the measurement  
6 circuitry 312 for output as part of the high definition  
7 output video signal S'. Finally, in the event that such  
8 timing signals correspond to portions of a high resolution  
9 display frame outside the intended display areas in these  
10 four quadrants (such portions are labeled E in Fig. 1), the  
11 control circuitry 318 cooperates with the switch 324 to  
12 read out the background video signal generated by the  
13 signal generator 314 for output as part of the high  
14 definition output video signal S'. In this manner, the  
15 high definition component signals (e.g., RGB signals)  
16 produced at the output of the switch 324 together with high  
17 definition timing components produced by the timing signal  
18 generator 316 provide the high definition output video  
19 signal S', which is suitable for display on a high  
20 definition display device to create a display of the form  
21 shown in Figure 1. Such control operations multiplex the  
22 picture component signal, the waveform/audio/vector  
23 displays and the background signal together to form the  
24 high resolution output video signal S' whereby the picture

1 component signal and the waveform/audio/vector displays are  
2 superimposed onto background signal to create a display of  
3 the form shown in Fig. 1.

4

5 In the illustrative embodiment shown in Fig. 3, the  
6 high resolution output video signal S' is represented by  
7 five distinct analog waveforms (R/G/B component waveforms  
8 and Hsynch/Vsynch timing waveforms). Alternatively, other  
9 high resolution analog signal formats, such as YPbPr and  
10 DVI-Analog, may be used. In these embodiments, the readout  
11 circuits 320, 322 perform digital-to-analog conversion and  
12 serialization of the digital pixel data values generated  
13 and stored by the resize circuitry 310 and measurement  
14 circuit 312, respectively. In alternative embodiments, the  
15 high resolution output video signal S' may be represented  
16 by a high resolution digital signal format, such as DVI-  
17 Digital or HDMI. In these embodiments, the readout  
18 circuitry 320, 322 need not digital-to-analog conversion as  
19 the pixel data is carried in digital form.

20

21 There have been described and illustrated herein an  
22 embodiment of a video signal processor in accordance with  
23 the present invention. While particular embodiments of the  
24 invention have been described, it is not intended that the

1 invention be limited thereto, as it is intended that the  
2 invention be as broad in scope as the art will allow and  
3 that the specification be read likewise. It will therefore  
4 be appreciated by those skilled in the art that yet other  
5 modifications could be made to the provided invention  
6 without deviating from its spirit and scope as claimed.